Amendments to the Specification

Please amend the title of the application to read:

"DECODER SYSTEM CAPABLE OF PERFORMING A PLURAL-STAGE PROCESS"

On Page 1, line 2 (after the title of the application), please insert the following new heading and paragraph:

CROSS-REFERENCE TO RELATED APPLICATIONS

This patent application is a divisional application of U.S. Serial No. 09/381,010, filed on September 13, 1999, which is the U.S. National Stage of PCT Application No. PCT/GB98/00917, filed on March 26, 1998, which claims priority to Great Britain Application No. 9706457.0, filed on March 27, 1997, and Great Britain Application No. 9713690.7, filed on June 30, 1997.

Please replace the first complete paragraph on page 42 (lines 1-5) with the following amended paragraph:

A first addressing scheme is described in the case where t=2 and n, the number of driver lines, is at least 7. Another parameter w is now associated with n, and defined such that: ~~w=[n – 3/4]~~ w=int((n-3)/4). The number N of output nodes in our addressing scheme is equal to 2nw and for each n, is at least as large as the integer $n^2/2-3n$. This is within 5n/2 of the maximum possible number $\binom{n}{2}$ of display electrodes in a scheme with n driver lines with c=2 and v=1. There is the additional advantage that any consecutive pair of display electrodes may be simultaneously addressed.

Please replace the last paragraph on page 43 (lines 25-29) with the following amended paragraph:

Next ~~we describe~~ the calculation process to be carried out by the address decoder is described. The input is the number of a display electrode to be activated, and the output is an activation pattern (equivalently, a pair of numbers in the range 0, 1,... n-1 corresponding to driver lines). Let D be the number of a display electrode, where $0 \leq D < 2nw$. Integer D is input to the address decoder. Then:

Please replace the fourth paragraph on page 44 (lines 10-12) with the following amended paragraph:

Finally for this scheme, it is described how an address decoder can calculate the activation pattern required to activate two consecutive display electrodes ~~and D+1~~ D and D+1, where $0 \leq D < 2nw-1$.

Please replace the last paragraph on page 44 (lines 27-30) with the following amended paragraph:

An addressing scheme is now described in the cases where t=3 or t=4 and n, the number of driver lines, is at least 9. The parameter w is again used, but is now defined as ~~w=[n - 3/6]~~ w=int((n-3)/6). The number N of output nodes in our addressing scheme is equal to 2nw and is roughly as large as the integer $n^2/3$.

Please replace the third paragraph on page 46 (lines 13-14) with the following amended paragraph:

- Let j with $0 \leq j < 2n$ and i with $0 \leq i < w$ be the unique integers with D=2ni+j. In fact, ~~i=[D/2n]~~ i = int(D/2n) and j = D mod 2n.

Please replace the fourth paragraph on page 47 (lines 12-15) with the following amended paragraph:

- If i =1 mod 3, then connect output numbered [[D]]D to the driver lines numbered m+i and to the driver line numbered by the j-th integer in the list:

  0, 1, 2,..., t-2, 3t-3, 3t-2,..., m-2, m-1, t-1, t,..., 2t-3.